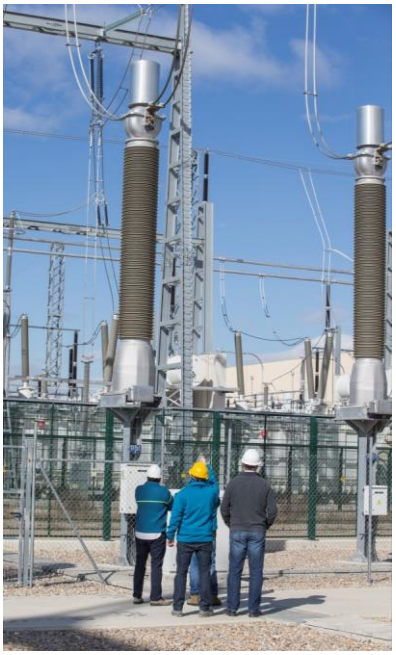

Bus and Breaker Failure Protection

SEL UNIVERSITY

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Technical literature supporting this section:

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- B. L. Qin, A. Guzmán-Casillas, and E. O. Schweitzer, III, "A New Method for Protection Zone Selection in Microprocessor-Based Bus Relays," *IEEE Transactions on Power Delivery*, Vol. 15, No. 3, July 2000, pp. 876–887.
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- A. Guzmán, B. L. Qin, and C. Labuschagne, "Reliable Busbar Protection With Advanced Zone Selection," *IEEE Transactions on Power Delivery*, Vol. 20, No. 2, April 2005, pp. 625–629.

- S. Briscombe, G. Lewis, and M. Thompson, “Stanford University, Palou Substation Modernization Project,” proceedings of the 31st Annual Western Protective Relay Conference, Spokane, WA, October 2004.
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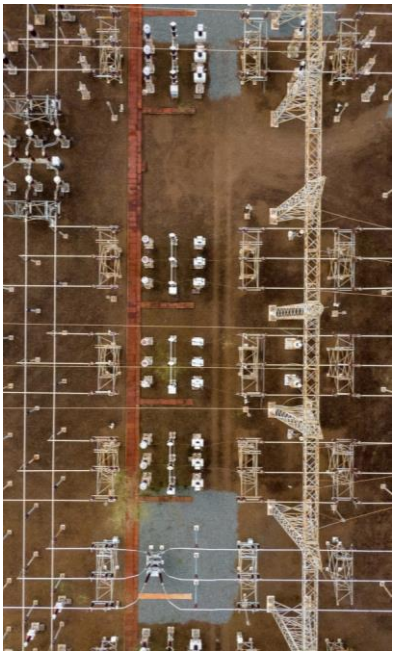
- IEEE Std C37.119, *IEEE Guide for Breaker Failure Protection of Power Circuit Breakers*, 2005.

Objectives

1. Discuss bus protection considerations and schemes
2. Discuss breaker failure protection considerations and schemes



Bus protection

System impact of bus faults

- Station equipment damage
- Thermal and mechanical stresses on network elements feeding the fault
- Power system transient instability
- Voltage collapse
- Power quality problems
- Personnel safety risk

A bus is a critical junction in an electric power system where many power system circuits converge. Unlike a distribution or transmission line fault disturbance, a bus fault disturbance can be very disruptive, primarily for two reasons. The first reason is that the convergence of supply circuits at the bus junction, particularly at transmission voltage levels, would supply high magnitudes of fault current to feed any bus fault. This high-current bus fault disturbance stresses the supply circuits converging at the faulted bus, and it can cause severe and costly damages to bus equipment, power system transient instability, and service disruption to customers or distribution networks. A fault at a critical bus that is left unmitigated for a long enough time, or beyond a certain "critical fault clearing time," can result in a wide-area blackout.

Second, clearing a faulted bus often must open up multiple branches of the power system, which can disconnect loads and reduce power transfer capability. This is certainly a more minor and desirable disruption when compared to the consequences of leaving a standing bus fault unmitigated.

Another serious consequence is the probability of human casualties, where the individuals most at risk are the substation technicians, contractors, and maintenance personnel.

Bus protection considerations

- Bus configuration and operational flexibility – fixed or switchable (reconfigurable)
- Availability and characteristics of CTs
- Availability of VTs
- Availability of auxiliary contacts of circuit breakers and disconnect switches (for switchable bus arrangements)
- Redundancy

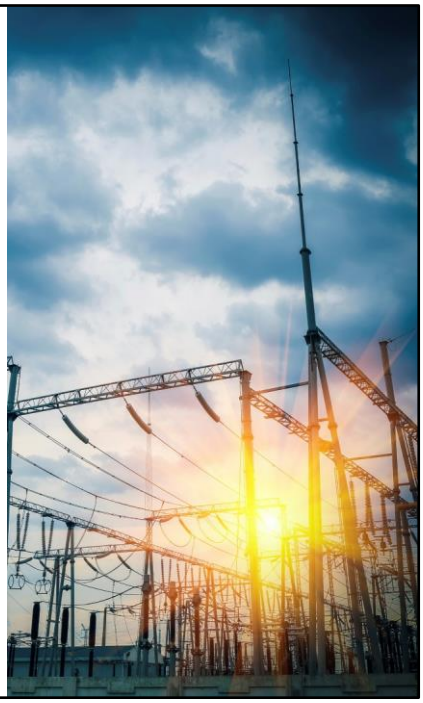
Which bus protection method you choose depends on if the bus configuration is fixed or switchable and if the current transformers (CTs) already in service have equal or different CT ratios and standard voltages. In switchable bus applications, differential protection schemes require information about the auxiliary contacts status of circuit breakers and disconnect switches to create a replica of the bus configuration.

Bus protection methods that use directional elements would require voltage transformers (VTs) for polarizing the directional elements. Furthermore, VTs provide additional security to differential protection schemes for switchable bus arrangements—differential current without an associated change in voltage indicates a dynamic bus replica error instead of a fault on the bus.

In the past, bus protection systems were often not redundant. Remote backup was considered adequate, because remote overreaching elements that could see an end-of-line fault could also see a fault on the bus. Traditional bus differential protection systems required dedicated CTs to be connected in parallel to sum the currents for obtaining the operating quantity; hence implementing dual high-speed protection for the bus zone was difficult. However, the safety considerations today make it more prevalent for high-speed bus protection to be redundant.

Bus protection considerations

- Performance requirements for specific application
  - Speed
  - Security
  - Selectivity
  - Sensitivity
- Cost and complexity



Bus protection should provide high speed and selective disconnection of the faulted bus. Sensitivity for internal faults is usually not a chief concern due to high bus fault currents; however, the selected bus protection method must provide high security for external faults.

The costs of implementing bus protection are generally commensurate with the size, layout, and complexity of the substation.

Bus protection requirements

- High-speed operation for all bus faults
- Security for external faults with heavy CT saturation
- Security during normal switching conditions
- Minimum operating time for external-to-internal evolving faults

The ideal bus protection scheme must perform to the requirements specified on the slide.

Different bus protection schemes will be discussed and compared later in this section.

Common bus arrangements

- Single bus with single breaker
- Double bus with bus tie breaker
- Main bus and transfer bus with single breaker (switchable)
- Double bus with single breaker (switchable)
- Breaker and a half
- Double bus with double breaker
- Ring bus

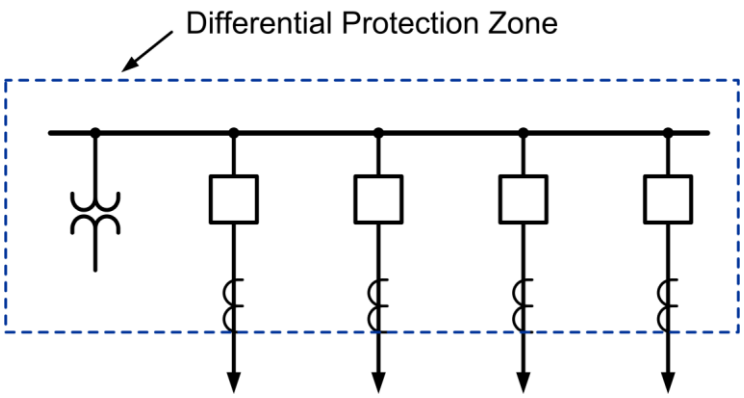
Bus configuration strongly influences bus protection system design. For protection, consider two major categories of bus configurations: fixed buses and switchable buses. In fixed bus configurations, the connection of branch circuits to buses is fixed. Zones of protection do not need to be reconfigured. In switchable bus configurations, branch circuits can connect to more than one bus by disconnect switches. These configurations require bus protection zone reconfiguration. In the past, zone reconfiguration required switching CT secondary circuits and/or breaker trip circuits. Microprocessor-based differential relays include zone reconfiguration abilities that allow static connections of CT secondary circuits and breaker trip circuits with the relay, thus avoiding the need to switch these circuits.

The bus configurations on the slide are the major ones in common use. Some important considerations in designing a bus include the following:

- Reliability requirements dictating whether to trip the whole bus or a section of it due to a bus fault
- Equipment maintainability and network switching flexibility
- Economical and footprint (space) constraints
- Sectionalizing requirements to avoid exceeding breaker fault duty and operational cycles
- Ease of future bus expansion

In the subsequent slides, five bus arrangements and their associated zones of protection are briefly covered. Refer to IEEE C37.234 for a more comprehensive discussion on bus arrangements.

Single bus with single-breaker configuration

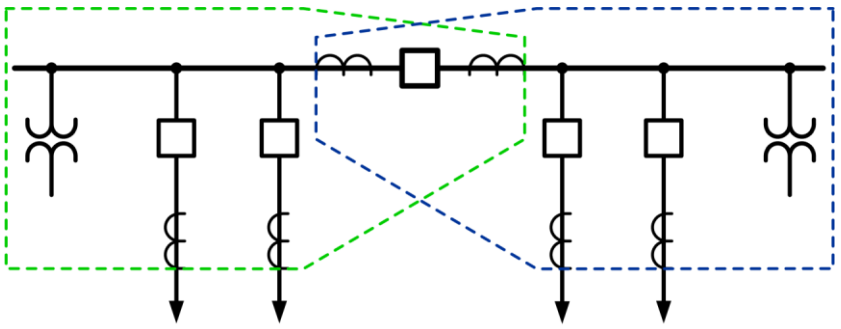


The single bus with single-breaker configuration consists of a single bus with all network elements connected directly to the breakers, as shown on this slide. This is a simple and economical bus configuration (also called a straight-bus configuration). But from a system point of view, it is the least reliable and flexible.

A single bus with single-breaker configuration is unreliable because all connected breakers trip for a bus fault, resulting in the disconnection of the entire station. To increase reliability and reduce breaker fault duty requirements, a single bus can be split into two (typically independently sourced) sections, with a switching device between them.

Lower operational flexibility results from removing a breaker from service for maintenance or interrupting service to the branch circuit when repairing a breaker. To increase flexibility, a single bus can be converted into a single bus and transfer bus with single-breaker configuration by adding a transfer bus and a transfer breaker.

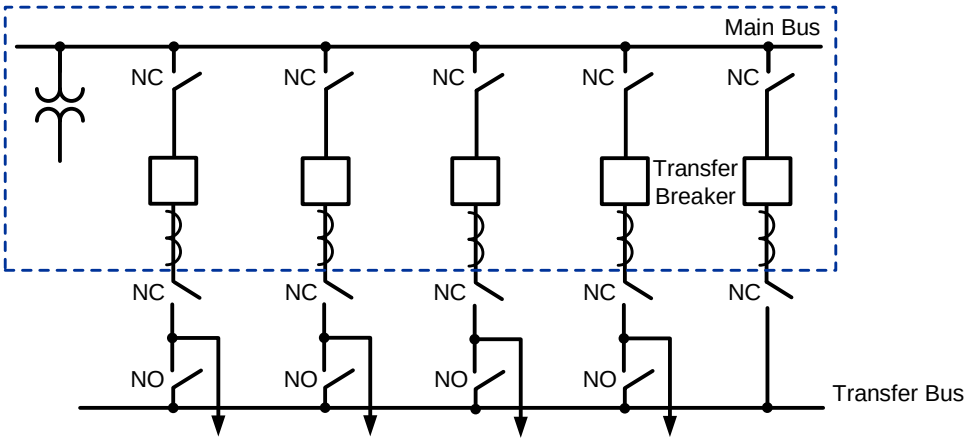
Double bus with tie-breaker configuration



The double bus with tie-breaker configuration shown on this slide is used in utility and industrial distribution buses. A bus-tie breaker divides the bus in two sections and may operate normally closed or open. Separate bus protection zones are required for the bus sections.

The overall substation reliability is increased, compared to the single-bus–single-breaker configuration, because faults on one of the bus sections only require tripping the faulted section. The other bus sections remain in service; however, operational flexibility remains the same as in the single bus with single-breaker configuration, because removing a breaker from service interrupts service to its branch circuit.

Main bus and transfer bus with single-breaker configuration



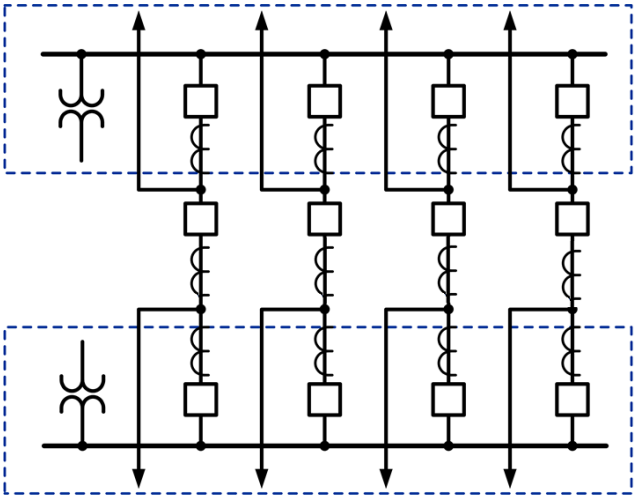
The main bus and transfer bus with single-breaker configuration shown on this slide is preferred by many companies at subtransmission levels.

The bus protection zone is allocated in a similar way as a simple-bus substation. The operational flexibility increases in comparison to the single bus with single-breaker configuration, because it is not required to remove a branch circuit from service when one of the breakers is taken out for maintenance.

The transfer breaker may be normally open or closed, depending on the utility practice. In any case, it does not provide any contribution to a bus fault. However, it must be included in the protection zone so that the bus remains protected when a branch circuit breaker is open and the transfer breaker is closed. When the transfer bus is in service, it is protected by branch-circuit protection and does not have a separate bus protection scheme.

The transfer breaker replaces the out-of-service breaker. The relay associated with the transfer breaker should functionally replace the relay of the out-of-service breaker. A good practice is to use a relay with multiple settings groups that allows replicating the settings of all the branch circuit relays.

Breaker-and-a-half configuration

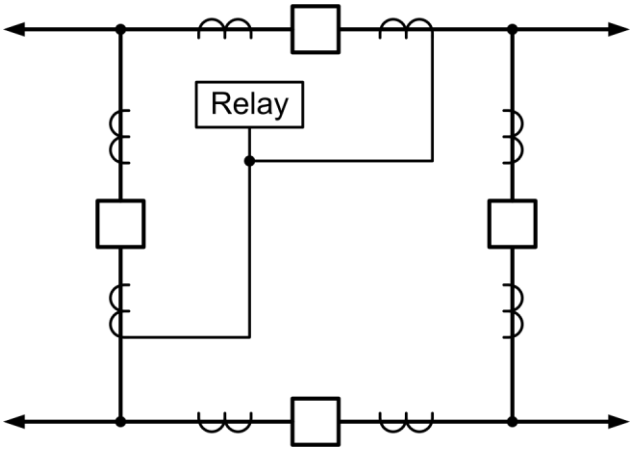


The breaker-and-a-half configuration shown on this slide consists of two bus sections connected by rows (bays). It has three breakers per row, along with two branch circuits tapped from each row; as a result, three breakers need to connect to only two branch circuits. In other words, the configuration has one breaker and a half of another per branch circuit (which is how the bus configuration got its name). This configuration is flexible, reliable, and relatively economical, especially when compared to other arrangements, such as a double bus with double-breaker configuration that calls for two breakers per branch circuit.

In the breaker-and-a-half arrangement, each bus has its own differential protection zone. The portion of the bay not protected by differential protection is protected by the line or transformer protection attached to that bay.

This bus arrangement is very resilient when there are at least three rows connecting the two buses together. This creates multiple paths for network elements to remain interconnected even when various circuits are open. It is relatively economical, because it requires only one extra breaker per two network elements. This arrangement can be made more economical when network elements that rarely trip (such as a transformer) are directly connected to the bus without a breaker. In that case, the bus zone and transformer zone are separated at the transformer bushing CTs. For faults in either zone, both zones are cleared. Often, there is an automatic restoration scheme that automatically isolates the transformer and recloses the bus breakers if the transformer zone relays trip.

Ring-bus configuration



In the ring-bus configuration shown on this slide, each bus section is protected by the branch circuit scheme connected between the pair of breakers; hence, this bus configuration does not require a dedicated protection scheme, except when the network element is a transformer. In that case, it is recommended to separate the transformer and bus zones at the transformer bushing CTs.

A ring bus is economical, because it requires the same number of breakers as a single bus with single-breaker configuration; however, ring buses with more branch circuits have lower resilience to breaker trips and the bus ability is reduced, weakening network paths that interconnect the branches once the ring is open.

Bus protection methods

- Differential protection
- Partial differential protection
- Zone-interlocked protection
- Arc-flash (light sensing) protection
- Fault-bus protection
- Protection using remote time-delayed relays

Bus protection must provide fast operation for all bus faults and high security for external faults. The slide shows the major types of bus protection schemes.

Differential protection, the best bus protection principle, operates on the sum of the currents entering the bus, also called the differential current. The relay trips the bus when it detects a differential current.

Partial differential protection, a subcategory of differential overcurrent protection, provides bus protection where not all of the branches connected to the bus include CTs.

Zone-interlocked protection uses signaling from the branch circuit relays to indicate whether a fault is inside or outside the bus zone. Zone-interlocked schemes include simple blocking (also known as fast bus tripping) schemes, suitable for radial buses, and directional comparison blocking (DCB) schemes, suitable for applications with sources on multiple branch circuits.

Fault-bus protection responds to the ground fault current flowing through the conductor used for grounding the enclosure of some metal-clad switchgear installations.

Time-coordinated relays that overlap the bus zone provide time-delayed protection for buses without a dedicated protection system. Clearing the bus fault requires tripping the remote ends of all lines with sources. Often, the bus protection system is not redundant, so this scheme also provides backup to the primary bus protection system.

Differential protection

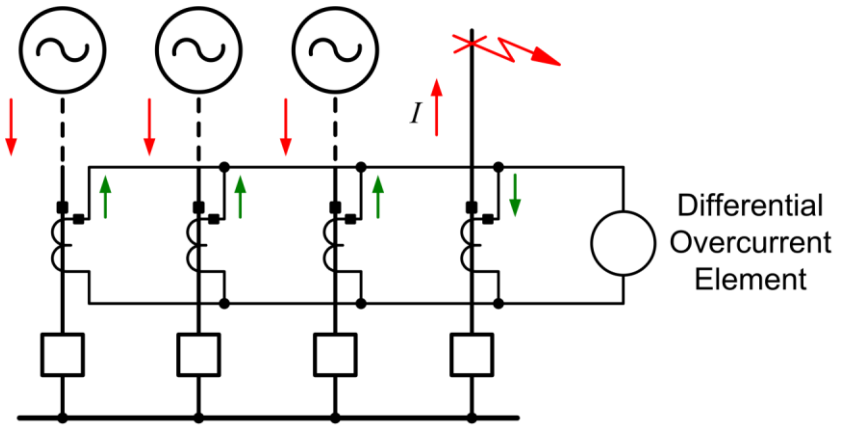
Differential overcurrent protection

High-impedance differential protection

Percentage-restrained (low-impedance) differential protection

Differential protection is often applied in bus protection for its high selectivity and high speed of operation. There are different types of differential relays/schemes, as shown on the slide, and each has a different level of performance with regard to speed, selectivity, sensitivity, and security. The zone of protection is determined by the location of the CTs and positions of the disconnect switches (for reconfigurable buses). For bus protection, high sensitivity is generally not particularly critical due to high minimum available fault current levels during a bus fault—except in high-impedance-grounded systems where the minimum available fault current levels are very low for ground faults.

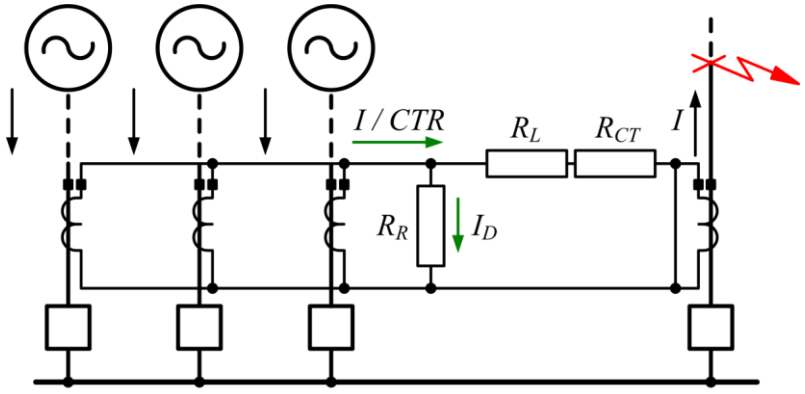
Differential overcurrent protection



A differential overcurrent protection scheme consists of an overcurrent element connected to the paralleled CTs in each phase, as shown on the slide. The differential current measured by the relay equals the sum of all the bus terminal currents. For an external fault, this current is zero under ideal conditions. For a bus fault, the differential current equals the fault current referred to the CT secondary.

The differential current resulting from unequal CT saturation can cause undesirable relay operation for external faults. During an external fault, the CT of the faulted branch circuit measures the total fault current, while the other CTs measure only the individual current contributions. These different CT current levels, added to possibly different CT types, burdens, and levels of remanence (magnetic flux trapped in the CT core), can cause unequal CT saturation.

Differential overcurrent protection



CT saturation creates
false differential current

$$I_D = \frac{R_L + R_{CT}}{R_L + R_{CT} + R_R} \bullet \frac{I}{CTR}$$

In a differential overcurrent scheme, the worst-case scenario for an external fault occurs when the CT on the faulted branch circuit saturates completely, while the other CTs remain unsaturated. This situation is illustrated on the slide, where the magnetizing impedance of the fully saturated CT becomes a short circuit. The parallel connection of the unsaturated CTs delivers a current equal to the total secondary fault current, which divides into two components: one component flows through the saturated CT and the other component, which is a differential current, flows through the relay branch—the equation is shown on the slide, and its quantities are defined as follows:

- I_D is the differential current caused by the saturated CT
- R_L is the resistance of the conductors connecting the saturated CT with the summing junction of the CTs
- R_{CT} is the secondary resistance of the saturated CT
- R_R is the relay element resistance plus the lead resistance from the summing junction of the CTs to the relay
- I is the external fault current (in primary amperes)

This false differential current can cause a misoperation of the relay and is thus a security risk. The equation shows that increasing the resistance of the relay branch (R_R) of the circuit and decreasing the values of the lead resistance (R_L) and CT secondary resistance (R_{CT}) reduces this differential current. Sometimes the CTs are paralleled in a summing junction box, and the single pair of leads is brought into the substation control enclosure. It is typically recommended that this summing junction box be located at a point close to and equidistant from each CT to minimize the value of R_L.

Differential overcurrent protection

Security enhancement methods

- Set pickup above anticipated worst-case differential current for external faults
- Use short inverse-time overcurrent element instead of instantaneous overcurrent element
- Insert burden resistor into differential branch of CT circuit to reduce differential current for external faults

A simple differential overcurrent scheme is not inherently secure. The methods outlined on the slide enhance scheme security. The first method has the disadvantage of reducing scheme sensitivity for internal faults. For the second method, the time delay of the element should be set to ride through the differential current caused by CT saturation until the CT recovers. The disadvantage here is that operating speed is sacrificed for security.

The third method involves using the differential element in series with an impedance that is sized to reduce the current that flows in the differential operate path during an external fault to below the pickup of the differential overcurrent element plus margin. This impedance is generally small enough so that an internal fault will not result in the development of significantly high voltages in the CT circuit.

Traditional approaches use the differential overcurrent scheme to reduce cost. However, the engineering analysis required to apply the scheme offsets its perceived low cost. We do not recommend the differential overcurrent scheme because of the relatively low cost of modern multifunction bus protection relays.

Differential overcurrent protection

Accuracy Class C CT selection

Avoiding saturation for maximum asymmetrical fault

$$I_f Z_b \left(\frac{X}{R} + 1 \right) \leq 20$$

where

- I_f is maximum fault current in per unit of CT rating
- Z_b is CT burden in per unit of standard burden
- X/R is X/R ratio of primary fault circuit

The criterion to avoid saturation for the maximum asymmetrical external fault is given by the above relation. The equation, as shown, assumes zero remanence and a fully offset short-circuit current. The impedance burden would vary based on the CT connection and the fault type.

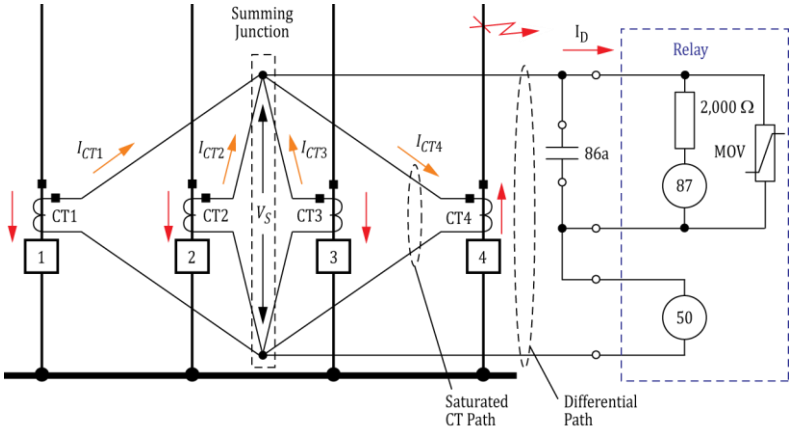
The relation is based on the ANSI standard C ratings and burdens. The ANSI standard burden is the resistance required to obtain the C rating voltage at 20 times the nominal current (8, 4, 2, or 1 ohm depending on the C rating of the CT).

The formula can also be used for IEC Class P CTs by equating the limiting voltage to the ANSI C rating. The value to be used for the standard burden can be calculated by dividing the limiting voltage by 20 times the nominal current rating of the CT secondary.

Saturation may still occur, even if this equation is satisfied, because the level of remanence in the CTs around the bus is very random. On the other hand, saturation may not occur after all if this equation is satisfied.

Additionally, this equation cannot be used to determine the amount of fictitious differential current caused by CT saturation for any given installation. Fortunately, all the differential protection methods can tolerate a certain level of fictitious differential current due to CT saturation. Differential overcurrent schemes achieve this with either a high setting or time delay. Other differential protection methods use high impedance or restraining techniques to remain secure when CTs saturate.

High-impedance differential protection



The high-impedance differential scheme introduces a high-value resistor (also called a stabilizing resistor) in the differential branch of the circuit to reduce the differential current resulting from the heavy CT saturation during external faults. The value for the resistor can be anywhere from 1,600 to 2,000 ohms. The diagram on the slide shows a typical application, which basically operates as follows:

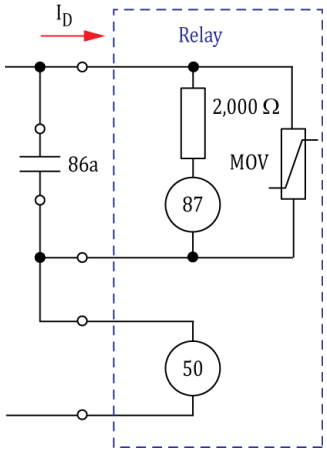
1. A low-impedance overcurrent element (87) senses the current flowing through the stabilizing resistor. The current through the 87 element is proportional to the voltage V_S across.
2. If CT saturation occurs for an external fault, the high impedance of the relay will force the current through the lower impedance path of the saturated CT. Very little current will then flow through the 87 element. For this current, the relay will not operate.
3. For internal faults, the significant current flowing through the 87 element causes the relay to operate; the resulting high voltage across the relay typically drives all CTs into saturation.

For internal faults, the voltage produced by the CTs to drive the differential current through the stabilizing resistor can reach dangerous levels. The relay circuit introduces a voltage limiter, such as a metal-oxide varistor (MOV), to limit this voltage to a safe level. Damage to the circuit can be prevented by shorting the stabilizer and the MOV with an auxiliary lockout relay contact (86a) to limit the energy absorbed by these components during an internal fault.

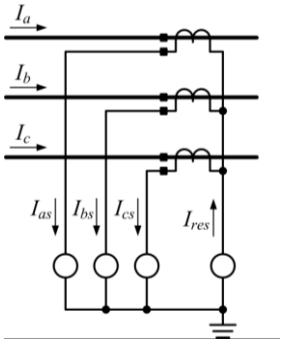
The scheme includes an optional instantaneous overcurrent element (50). Use this element when a sustained breaker failure initiation (*BFI*) signal is required. When the 87 element operates and trips the lockout relay, the high-impedance path is shorted and the 87 element drops out. The differential current will continue to flow until all breakers successfully interrupt the fault, so the 50 element remains asserted and sustains the *BFI* signal. The 50 element can also improve scheme dependability by allowing a trip condition if an MOV failure short-circuits the high-impedance path when high voltage is present.

High-impedance differential protection

Calculating secure voltage setting



$$V_{PU} = K_S \bullet \left(n \bullet R_L + R_{CT}\right) \bullet \frac{I}{CTR}$$



The scheme requires dedicated CTs on all bus terminals. For security, set the relay voltage pickup above the maximum expected voltage at the CT summing junction for an external fault with total saturation of the faulted branch circuit CT. The equation on the slide gives the relay voltage pickup setting, V_{PU}. The equation quantities are defined as follows:

R_L is the resistance of the conductors connecting the summing junction with the most distant CT.

R_{CT} is the CT secondary resistance.

I is the maximum external fault current.

K_S is the security factor (typically 1.5 to 2).

n is 1 for three-phase faults and 2 for single-phase-to-ground faults (with wye-connected CTs).

The right-side figure shows that, for wye-connected CTs, there is no neutral current for three-phase faults; the one-way conductor resistance R_L should be considered in the V_{PU} equation for three-phase faults (n = 1). For single-phase-to-ground faults, there is current returning through the neutral; the two-way conductor resistance $2R_L$ should be considered for single-phase-to-ground faults (n = 2 in the equation).

Since we have different n values and different fault current values for three-phase and single-phase-to-ground faults, it is recommended practice to calculate the relay setting for both fault types and then select the higher setting as V_{PU}.

High-impedance differential protection

Calculating dependable voltage setting

$$V_{PU} = K_D \bullet V_{STD}$$

where

- V_{STD} is accuracy class voltage of CT with lowest voltage rating
- K_D is security factor

To ensure dependable operation for an internal fault, set the voltage pickup value lower than or equal to the accuracy class voltage of the CT with the lowest voltage rating in the circuit, as shown by the equation on the slide. Industry guidelines recommend a K_D value of 0.5 to 0.67. If the resulting setting is smaller than the minimum V_{PU} setting in the equation on the previous slide, a higher value of K_D can be used (up to $K_D = 1$) to obtain a better balance between dependability and security.

To reduce the voltage pickup setting, minimize the R_L value in the equation for V_{PU} on the previous slide by paralleling the CT secondaries at the switchyard as closely as possible to the CTs. If the CTs are of adequate voltage rating to support the higher voltage setting and the lower sensitivity that results from this setting is acceptable, the summing junction does not need to be in the switchyard.

We recommend to use CTs with a voltage class equal to or greater than 200 V in the high-impedance differential protection scheme.

High-impedance differential protection

Checking sensitivity for internal faults

Minimum internal fault current to reach pickup voltage

$$I_{MIN} = (N \bullet I_E + I_{Relay} + I_{MOV}) \bullet CTR$$

where

- N is number of CTs
- I_E is excitation current at voltage setting
- I_{Relay} is relay current at voltage setting
- I_{MOV} is overvoltage protection current at voltage setting

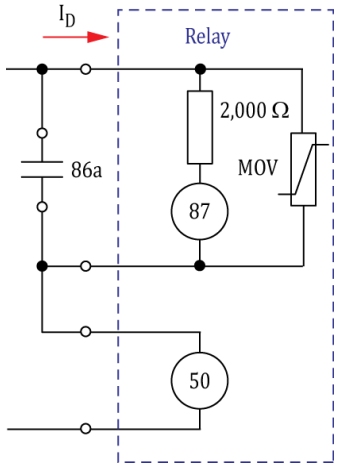
To check the relay sensitivity at pickup, calculate the minimum amount of internal fault current required to reach the pickup voltage. For low fault currents, such as those in high-impedance-grounded systems or during high-resistance ground faults, the current required to excite each CT to the voltage pickup level must be added to the current in the stabilizing resistor at the voltage pickup level and to the MOV current at the voltage pickup level (this MOV current is typically neglectable). The minimum internal fault current required to reach the pickup voltage is the sum of these currents, which is referred to the primary of the CT. The sensitivity of the voltage setting is considered adequate if the minimum internal fault current at pickup is less than the minimum expected internal bus fault current.

It is recommended practice to use the full ratio of all CTs to reduce the voltage in the circuit during an internal fault. If a CT is tapped at a partial winding, the high voltage on its connected terminals will be elevated by the autotransformer effect to an even higher voltage at the end terminal of the CT secondary winding. If equal ratio CTs are not available, this scheme can still be used but with special connections.

The high-impedance differential scheme is very sensitive because it takes only a small differential current flowing through the stabilizing resistor to produce voltage high enough to trip. This high sensitivity makes it generally suitable for application in high-impedance-grounded systems. When available CTs comply with the scheme requirements, the high-impedance bus differential scheme is a very effective and economical solution, especially for buses with many terminals and simple configurations.

High-impedance differential protection

Calculating 50 element pickup current



$$I_{PU} = K_I \bullet \frac{I_{F\ MIN}}{CTR}$$

As mentioned earlier, the scheme includes an optional instantaneous overcurrent element (50). This element provides a sustained breaker failure initiation (*BFI*) signal when required. When the 87 element operates and trips the lockout relay, the high-impedance path is shorted and the 87 element drops out. The differential current will continue to flow until all breakers successfully interrupt the fault, so the 50 element remains asserted and sustains the *BFI* signal. The 50 element can also improve scheme dependability by allowing a trip condition if an MOV failure short-circuits the high-impedance path when high voltage is present.

The 50 element pickup current must be set lower than the minimum bus internal fault current.

The equation quantities are defined as follows:

I_{PU} is the 50 element pickup current
$I_{F\ MIN}$ is the minimum bus internal fault current
K_I is the security factor (typically equal to 0.5)

Percentage differential protection

Basic operating principle

$$I_{OP} = \left|\bar{I}_1 + \bar{I}_2 + ... + \bar{I}_n\right|$$

$$I_{RT} = k \bullet \left(\left|\bar{I}_1\right| + \left|\bar{I}_2\right| + ... + \left|\bar{I}_n\right|\right)$$

$$I_{RT} = \max\left(\left|\bar{I}_1\right|, \left|\bar{I}_2\right|, ... \left|\bar{I}_n\right|\right)$$

Relay operates when

$$I_{OP} > I_{PU}$$

$$I_{OP} > SLP \bullet I_{RT}$$

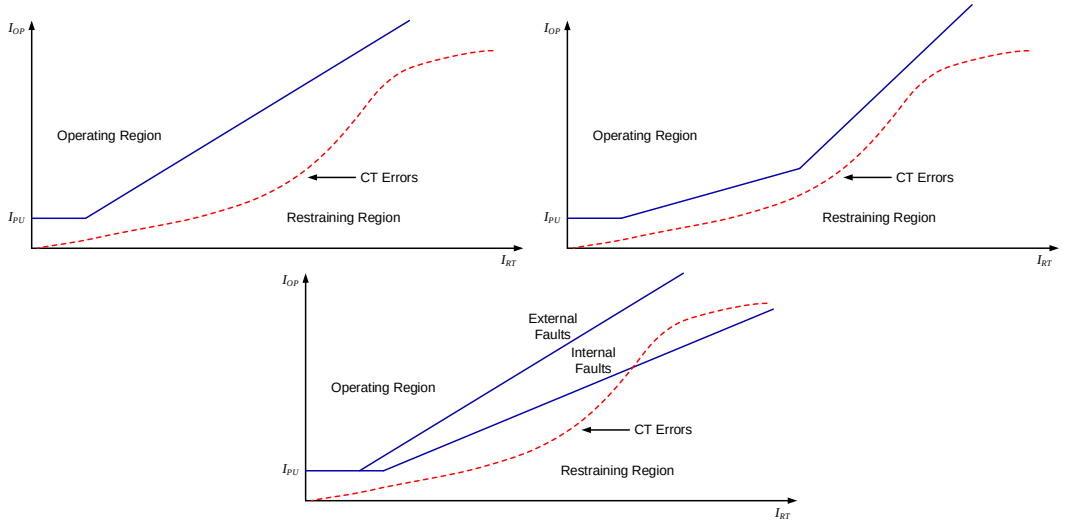
Modern percentage bus differential relays measure all the bus terminal currents (no CT paralleling necessary). A percentage differential element uses the top equation on the slide to calculate the operating (I_{OP}) current and one of the other two equations to calculate the restraining (I_{RT}) current. The percentage differential element generates a tripping signal if the operating current is greater than the minimum pickup current and is also greater than a certain percentage of the restraining current.

There are various definitions for the restraining current, as shown on the slide. The same slope setting will yield different sensitivities if different functions for the restraining quantity are used. Thus, it is important and beneficial to determine how the restraining current is derived before transferring settings between relays of different technologies, different generations, or from different manufacturers.

For the equations on the slide:

I_{OP} is the differential operating quantity.
I_{RT} is the restraining quantity.
k is a scaling factor, typically in the range of 0.5 to 1.
n is the number of terminals.
SLP is a relay slope setting.
I_{PU} is the minimum pickup current.

Percentage differential element characteristics



A percentage differential element generates a tripping signal if the operating current I_{OP} is greater than the minimum pickup current I_{PU} and is also greater than a percentage of the restraining current I_{RT}. This percentage is defined by the slope *SLP*, a relay setting.

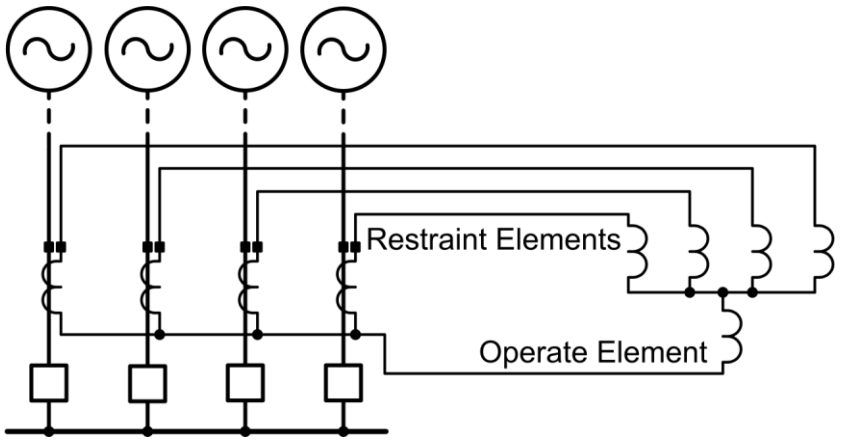
The upper left side figure on this slide shows the resulting single-slope operating characteristic as a scalar plot of I_{OP} as a function of I_{RT}. The characteristic is a straight line with a slope equal to *SLP* and a horizontal straight line defining the element minimum pickup current I_{PU}. The operating region is located above the characteristic, and the restraining region is below the characteristic.
The figure also represents the operating current resulting from CT errors for external faults. For low fault currents, the CTs behave linearly and the error current is a linear function of the restraining current. For higher fault currents, the CTs saturate and cause a nonlinear growth of the operating current.

The slope characteristic of the percentage differential element provides security for external faults that cause CT saturation.

Researchers have developed several methods to improve the sensitivity of the percentage differential element without sacrificing security. One method is the dual-slope differential characteristic (shown in the upper right-side figure), which further increases relay security for high-current external faults to accommodate CT saturation errors, thus allowing more sensitive settings. Some electromechanical differential relays had a nonlinear characteristic for this purpose.

The adaptive characteristic shown in the bottom figure is another method to improve sensitivity for internal faults and security for external faults. The single slope increases when the fault detection logic detects an external fault condition, adding security to the scheme.

Percentage differential protection



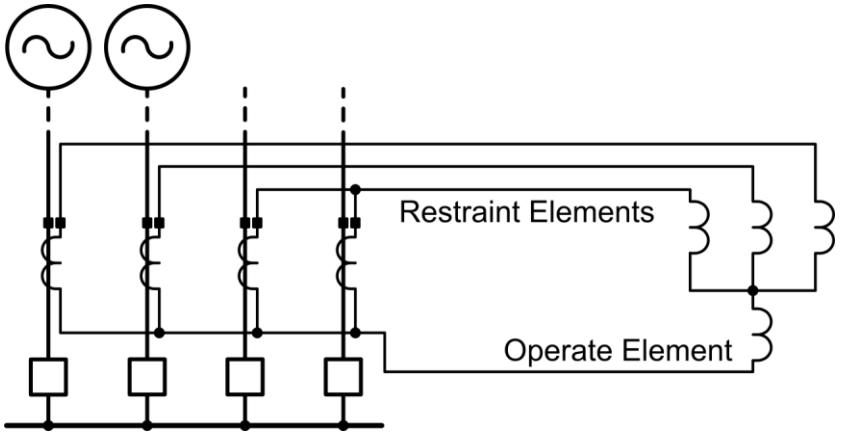
When the CTs have equal ratios, the high-impedance bus differential scheme described previously is very effective and economical. If the CTs are of different ratios or if the bus is a reconfigurable bus, the high-impedance scheme becomes less effective. Thus, a percentage differential scheme with multiple restraining circuits is recommended. Percentage differential elements compare an operating current with a restraining current.

Electromechanical percentage differential relays have several inputs, each connected to an individual internal auxiliary CT with variable turns (taps) to compensate for any ratio difference in the main CTs. With CTs of the same ratio, a nonsettable single slope is used and the relay taps are set the same. The tap selected is based on the available fault current and the CT ratio.

For external faults, current will circulate among the CTs through the restraining elements with little or no current flowing through the operating element.

For internal faults, the current will flow through the restraining element and the operating element.

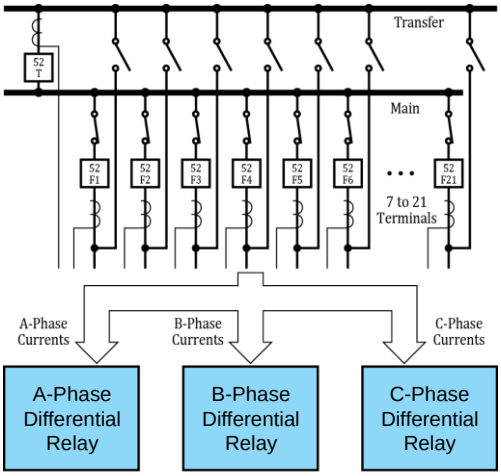
Percentage differential protection



The number of available restraint inputs is usually the main limitation of a multiple restraint differential relay. In the past, engineers traditionally paralleled CTs when the bus had more CT circuits than available restraint inputs. With the traditional percentage bus differential scheme, the paralleled CTs were the ones monitoring lines without sources. By only paralleling lines without sources, you minimize the opportunity for false differential current because of unequal CT response. However, this practice sacrifices security, because if one of the paralleled CTs saturates, it will not contribute adequate restraint.

Percentage differential protection

Use microprocessor-based bus differential relay to protect buses with as many as 21 terminals



Paralleling CTs is no longer necessary with the availability of modern bus differential relays. For example, a single modern microprocessor-based bus differential relay can provide as many as 21 analog current inputs. Therefore, one such relay can protect buses with as many as seven branch circuits or terminals. Two such relays can protect buses with as many as ten terminals (A-and B-phases are in one relay, and the C-phase is in the second relay). Furthermore, three such relays can protect buses with as many as 21 terminals.

The slide shows a sample connection for a microprocessor-based bus differential relay in a bus differential protection scheme involving 21 terminals.

Advanced bus differential protection

Preferred choice when

- CTs present saturation problems
- CTs are of different ratios
- CTs must be shared with other protection schemes
- Substation has complex (or switchable) bus arrangement

Traditional percentage differential relays lack security for external faults in substations with heavy CT saturation problems. High-impedance differential relays are difficult to apply with CTs that have low voltage ratings or dissimilar ratios. Advanced microprocessor-based bus protection systems solve these problems and are the preferred choice for the applications specified on the slide.

Advanced bus differential protection

Combining three elements

- Differential element using phasor values
- Directional element using phasor values
- Fault detection logic using instantaneous values

For the reasons mentioned earlier, advanced bus differential protection relays are highly recommended for bus protection. Depending on the relay manufacturer, the operating logic of an advanced bus differential protection relay may involve a combination of the following:

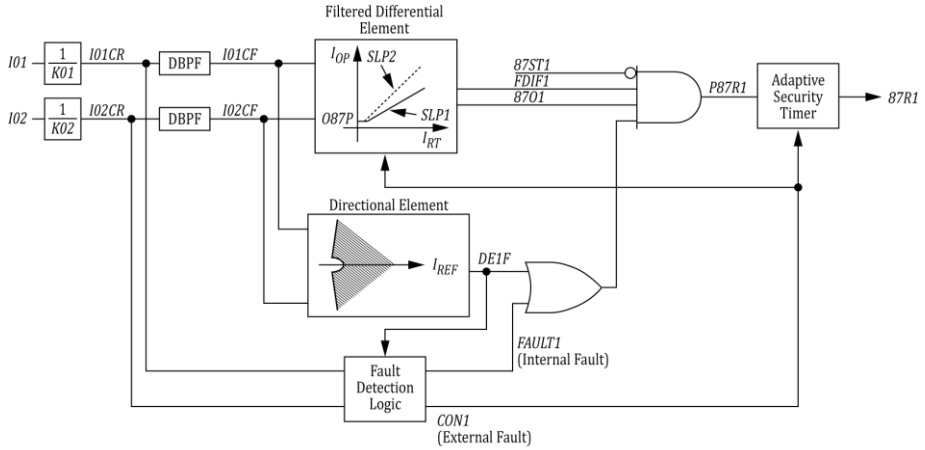
- Percentage-restrained differential function
- Directional function
- Overcurrent differential function
- External fault detection function
- CT saturation detection algorithm
- Level check for the differential and restraining currents

The compromise between security and dependability provided by an advanced bus differential relay varies among different relay manufacturers. To increase security, the relay may require the operation of the differential and directional elements, apply an automatic and temporary increase of the slope when an external fault is detected, and apply other solutions.

An example of an advanced bus differential relay is discussed in the following slides. In this relay, each bus zone is assigned to a bus protection relay element. This element consists of a differential element, a directional element, and fault detection logic.

Advanced bus differential protection

Zone 1 overall scheme



The differential element generates a tripping signal when I_{OP} is greater than the minimum pickup current, I_{PU}, and is also greater than a percentage of I_{RT}. The figure on the slide shows the adaptive differential element characteristics comprising two slopes: *SLP1* and *SLP2*. *SLP1* is effective for internal faults and *SLP2* is effective for external faults. The assertions of outputs *FDIF1* and *87O1* indicate that the operating point is in the tripping region of the filtered differential element characteristic.

The bus protection element logic also requires operation of either the directional element (*DE1F* assertion) or the internal fault detection logic (*FAULT1* assertion) to declare an internal fault (*P87R1* assertion). This fault declaration assumes that there is no CT trouble (*87ST1* is deasserted). The *P87R1* bit drives an adaptive security timer that controls the final output (*87R1*) of the bus protection element.

The fault detection logic controls the relay operating mode. During normal operating conditions, *CON1* is deasserted. For external faults, *CON1* asserts and switches the relay to a high-security mode where:

- The slope of the percentage differential characteristic changes from *SLP1* to *SLP2*.
- The instantaneous differential element (part of the fault detection logic) does not declare an internal fault unless the operating point stays in the tripping region of its characteristics during two consecutive half cycles.
- The delay time of the adaptive security timer increases.

Overall, this scheme provides high security for external faults and can detect internal faults in less than a cycle.

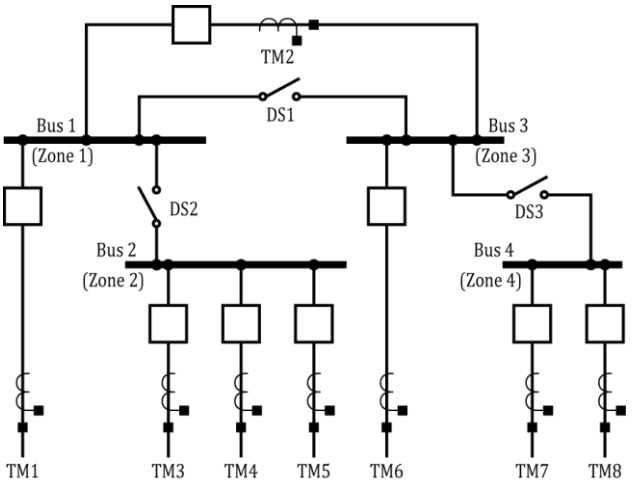
Adaptive slope increases security and sensitivity

- Adaptive slope allows for higher sensitivity without sacrificing security for external faults
- Relay detects external fault within 2 ms and switches to high-security mode
- *SLP1* can be set as low as 15%
- Relay can trip if fault evolves to internal (tripping not blocked)

An adaptive slope in the differential relay element provides higher security and sensitivity than that of elements with a fixed slope. Because the relay detects an external fault within 2 milliseconds and switches to high-security mode, *SLP1* can be set as low as 15 percent.

The security mode simply changes the slope setting to avoid tripping for an external fault but it does not block the relay from operating. The differential element is still enabled and ready to trip if the fault evolves into an internal fault. If the operating and restraining currents increase at the same time, the fault is internal and the relay trips as soon as the operating current exceeds the percentage restraint characteristic and the minimum operating current threshold.

Advanced zone selection logic



On the slide is an example of a reconfigurable bus arrangement with four buses and eight terminals. When switching operations can change the bus configuration, bus protection schemes must have zone-selection logic to dynamically adapt to these changes. Accurate zone selection ensures that the relay includes all terminals within the protection zone. Zone selection logic uses the station configuration information provided by the disconnect switch and the breaker auxiliary contacts. This logic assigns input currents to the appropriate differential element and determines the breakers to trip if a bus fault occurs.

The zone-selection logic essentially determines:

- The bus-zone(s) included in each protection zone
- The terminals included in each protection zone
- The terminals to trip for differential protection operation

Improving security in zone selection applications

- Voltage supervision
- Check-zone supervision

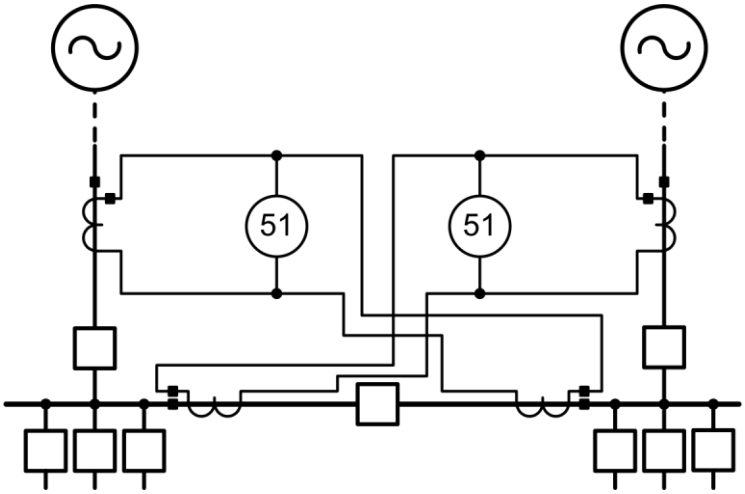
When zones dynamically adapt to the bus-switching topology, errors in the assignment of CTs to zones can cause differential elements to misoperate. These errors can occur temporarily because of timing differences between the actual disconnect switch state changes and the CT reassignment. Failure of a disconnect switch status contact used in the dynamic zone-selection logic can also cause errors. Two security solution methods for addressing these errors are voltage supervision and check-zone supervision.

When voltage supervision is applied to the differential tripping logic, differential operation is prevented when a differential element picks up but all bus voltages, as indicated by the zone VTs, are healthy.

The check-zone method uses a check zone to supervise the bus zones. A check zone is a differential zone defined by the bus branch circuits at the external boundaries of the dynamically switched zones. Check-zone CTs are never switched and are thus unaffected by dynamic zone-selection errors. If one of the dynamically selected zones measures differential current but the check zone does not, a zone selection error rather than a bus fault is the cause of the differential current.

Check-zone supervision can reduce bus protection dependability in some situations. One example situation is when a bus fault occurs in a substation with a double-bus-single-breaker configuration, where the bus-tie breaker is open. The check-zone supervision may overrestrain and prevent the correct operation of the bus differential protection zone element. Hence, the bus differential scheme should be able to override check-zone supervision when the tripping zones inside the check zone become electrically separated.

Partial bus differential protection



Partial differential protection schemes use inverse-time overcurrent relays fed from paralleled CTs that monitor only the sources to the bus. Each relay provides primary protection to its corresponding bus section and backup protection to the feeders connected to this bus section. Therefore, each overcurrent relay must coordinate with the overcurrent relays of these feeders. The result is time-delayed bus fault clearing.

Partial differential protection schemes are used when not all bus branch circuits have CTs available to provide a complete differential zone. Previously these schemes were also used when feeder CTs had different CT ratios and/or characteristics than the CTs installed in the source circuits and the bus-tie breaker, making the feeder CTs unsuitable for differential protection. However, modern microprocessor-based relays can tolerate a ratio mismatch and can be applied in this scenario. Partial differential schemes are better confined to backup protection.

Fast bus tripping schemes that protect buses with main and tie breakers are simpler if the main tripping element responds to the partial differential currents. It is not necessary to block two tripping elements or to make the overcurrent element directional on the tie breaker.

Zone-interlocked protection

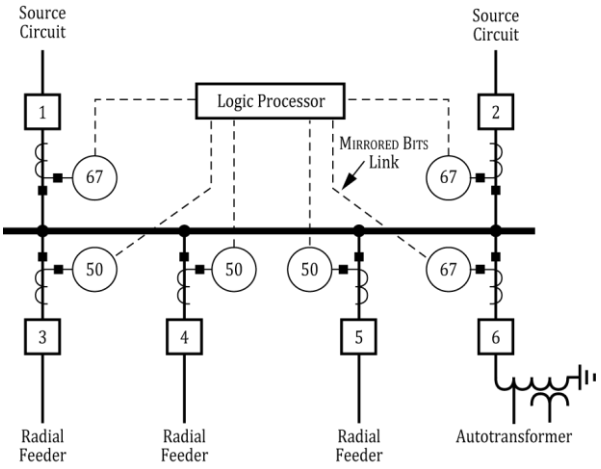
Directional comparison blocking scheme

Simple blocking scheme (fast bus tripping)

An alternative to bus differential protection is a zone-interlocked scheme, which uses information from the relays on each of the bus branch circuits to determine whether a fault is internal or external to the bus. Each relay sends status information on its branch circuit. For buses with multiple sources, the scheme requires directional relays on the source circuits. In radial systems, the scheme requires only overcurrent relays. To implement this scheme with existing devices, use the directional and overcurrent elements available in the branch circuit multifunction relays. The performance of this scheme is almost independent of the ratio, characteristics, and performance of the CTs. This substantial independence makes the scheme suitable for substations that have CTs of different types and/or ratios, especially when high operating speed is not required.

Zone-interlocked schemes are applicable only for single-breaker configurations.

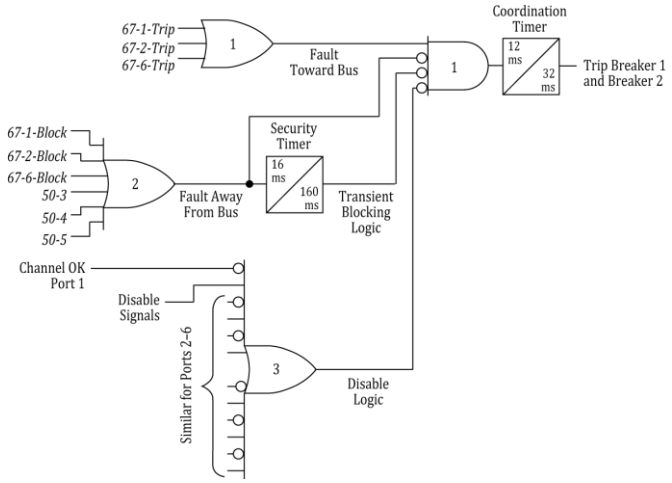
Zone-interlocked directional comparison scheme application



The figure on the slide shows an example of a directional comparison blocking (DCB) bus protection scheme and is explained as follows:

- Two source circuits and four load circuits (three of which are radial feeders) connect to the bus
- Directional overcurrent elements (67) protect the two source circuits; instantaneous overcurrent elements (50) protect the three radial feeders
- The fourth load circuit includes an autotransformer that is a zero-sequence source, so it uses a directional overcurrent element
- A logic processor, to which each relay connects, can be used to save and perform the bus protection logic

Zone-interlocked directional comparison scheme logic



The basic logic scheme primarily consists of three OR gates, the functions of which are described below.

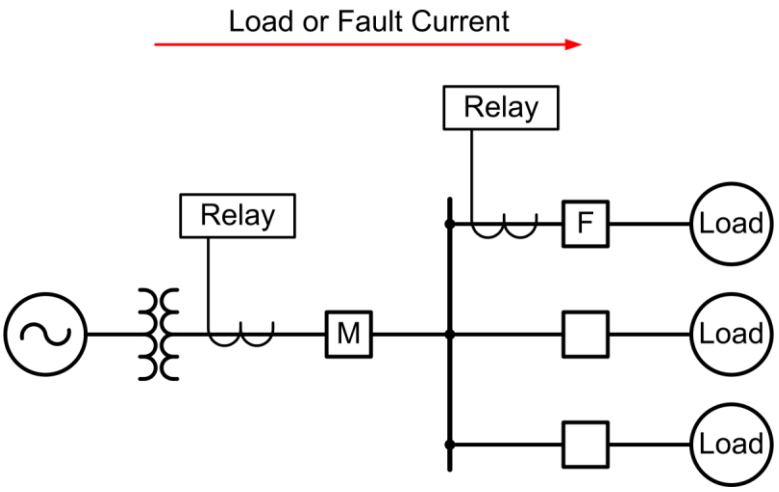
- OR Gate 1 receives the logic status of the directional overcurrent elements looking into the bus (tripping elements) at the source breakers (*67-1-Trip*, *67-2-Trip*, and *67-6-Trip*). This OR gate provides the Fault Toward Bus (tripping) output.
- OR Gate 2 receives the logic status of the blocking directional overcurrent elements at the source breakers (*67-1-Block*, *67-2-Block*, and *67-6-Block*) and the overcurrent elements at the radial feeder breakers (*50-3*, *50-4*, and *50-5*). OR Gate 2 provides the Fault Away From Bus (blocking) output.
- OR Gate 3 disables the scheme if communication is lost; that is, "Channel OK" becomes "0" in this case and results in the assertion of OR Gate 3. OR Gate 3 also receives disable signals from the branch circuit relays; these disable signals assert under two possible conditions:
  - Loss of potential at any of the directional relays at the source breakers. An LOP event can result in the loss of directionality, which ultimately compromises the security of the scheme.
  - Out-of-service relay testing. Disabling the DCB scheme here is essential to prevent spurious trips or fail-to-block problems when an external fault occurs on the branch circuit with the out-of-service relay.

Tripping occurs if any relay detects a fault toward the bus (or OR Gate 1 asserts) and no relay detects a fault away from the bus (or the OR Gate 2 output does not assert).

The coordination timer provides a communications coordination delay. The Fault Toward Bus logic must wait 12 ms to allow any blocking signal to arrive. The 32 ms dropout in the coordination timer ensures that the tripping signal is transmitted for the time required for tripping to occur.

The security timer prevents tripping when an external fault clears. If this timer receives a blocking signal for 16 ms, it holds its output asserted for 160 ms to prevent tripping if the blocking relay resets before the tripping relay.

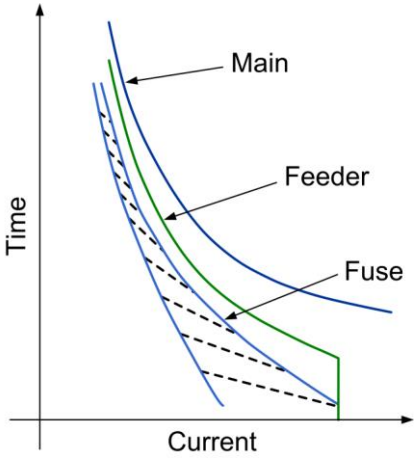
Radial distribution system



Consider the case of a simple radial system. A radial distribution substation can be defined as that having a single source. There are no sources of fault or load current on the feeders. For this system, current flows in one direction, from the source to the load.

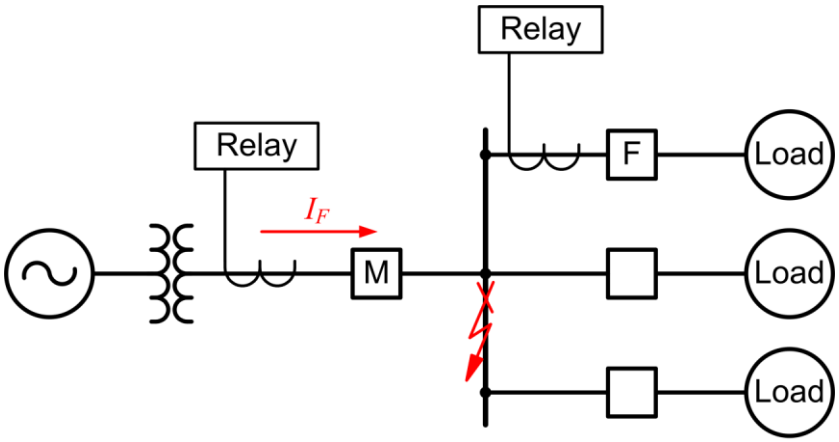
Traditional coordination of main and feeder overcurrent elements

Typical overcurrent coordination for downstream feeder fault



The figure depicts traditional phase coordination between the substation main breaker overcurrent relay, feeder overcurrent relays, and fuses.

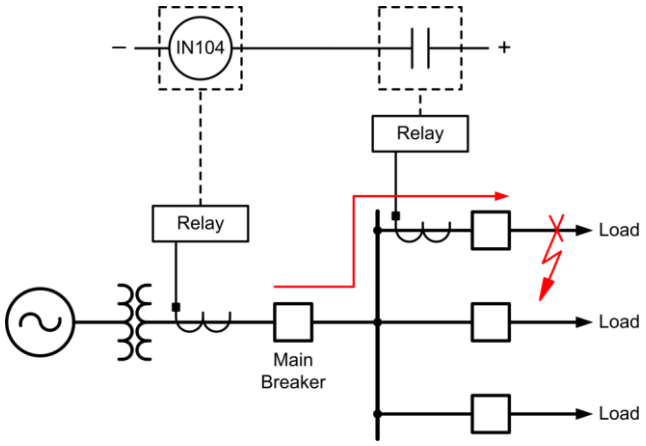
Traditional scheme clears bus faults with time delay



Bus faults are common at distribution levels because small animals can easily bridge the small clearances between grounded steel structures and energized buswork. The common practice is to clear bus faults with transformer backup protection, which has a time delay to coordinate with feeder protection. Fault clearing times are typically between 0.5 and 1.0 seconds. However, high fault current and the number and duration of bus faults can reduce the operating life of the power transformer, the most important and expensive element in the substation.

In radial substations, a simple and economical zone-interlocked blocking scheme, sometimes called a fast bus tripping scheme, provides relatively high-speed fault clearing for buses that do not have differential protection. Instead of relying on the traditional coordination interval in the bus main relay, this scheme requires only a short delay to allow the feeder relays to block the bus main relay for an external fault. The scheme can operate for bus faults in approximately 2 to 3 cycles.

Fast bus tripping scheme application

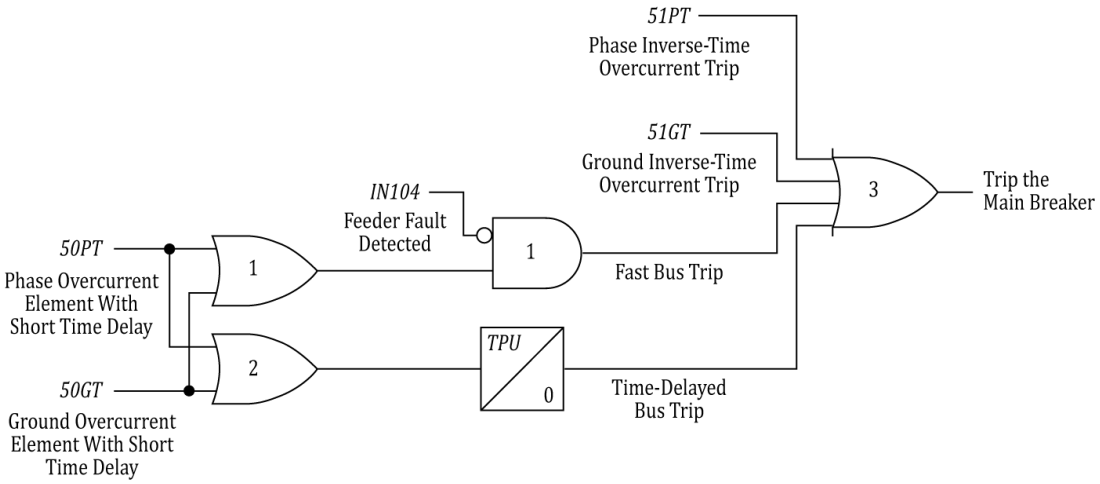


A fast bus tripping scheme can be implemented as follows:

1. Program an instantaneous overcurrent element in each of the feeder relays to close an output contact when a fault occurs on the feeder.
2. Wire the blocking contacts from each of the feeder relays in parallel to an input on the bus main relay.
3. Delay overcurrent elements in the bus main relay only long enough to allow sensing of the blocking contacts; a typical coordination delay is approximately 1 to 2 cycles.

A microprocessor-based relay greatly simplifies the wiring and equipment associated with the implementation of a fast bus trip scheme.

Fast bus tripping scheme logic



The slide shows the basic logic scheme, which is programmed into the bus main relay:

1. AND Gate 1 receives the logic status of phase and ground overcurrent elements, both of which include a short time delay. AND Gate 1 also receives the logic status of the relay IN104 input.
2. Fast bus trip occurs (AND Gate 1 output asserts) if the phase and/or ground overcurrent elements detect a fault (50PT and/or 50GT inputs assert) and no feeder relay detects the fault (IN104 input does not assert).
3. Time-delayed bus trip occurs (timer output asserts) if the 50PT and/or 50GT inputs remain asserted long enough for the timer to time out. This independent time-delayed trip provides backup when the scheme is disabled or a feeder breaker fails to operate for a feeder fault. Typical timer TPU delays are 12 to 30 cycles.

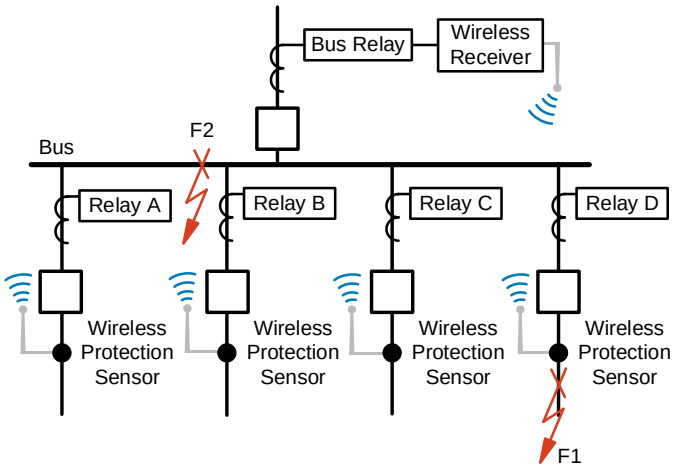
Set the pickup current of the instantaneous overcurrent elements in the bus main relay to detect the minimum bus fault with margin. For proper coordination, ensure that these elements are less sensitive than the instantaneous overcurrent elements in the feeder relays.

For the feeder fault shown on the previous slide, the scheme operates as follows:

1. The output contact of the feeder relay closes because of the feeder fault.
2. Input IN104 asserts in the bus main relay and prevents the AND Gate 1 output from asserting. No fast bus trip occurs.
3. If the feeder protection does not clear the fault quickly enough, the timer output asserts after a time delay TPU to trip the main breaker.

Phase and ground inverse-time overcurrent elements provide the traditional time-delayed backup protection. Set these elements with lower sensitivity and a longer time delay than the feeder overcurrent elements. For feeder or bus faults, 51PT and/or 51GT inputs assert after the corresponding time delay to initiate tripping of the main breaker.

Fast bus tripping scheme using wireless sensors



Fast bus tripping schemes work well when all the protective relays in the scheme can communicate block signals via hardwired connections between contact I/O or high-speed digital channels. There are, however, situations where hardwiring is not feasible and high-speed digital communication is not available.

A high-speed wireless protection sensor system can help in this situation. This system consists of a line-powered current sensor that detects fault currents and communicates this information to a receiver device. The fault detection and system communications latency are short enough to make the system viable for a fast bus tripping scheme.

The high-speed wireless protection sensors are installed on each feeder and communicate with the wireless receiver connected to the bus relay, as shown in the figure. A feeder fault (F1) is detected by both Relay D and the wireless sensor on the faulted feeder. Relay D trips for this fault, and the high-speed wireless protection sensor sends a fault indication signal to the wireless receiver confirming the feeder fault. This signal is used to block the fast bus tripping overcurrent elements on the main breaker.

When a bus fault (F2) occurs, no wireless protection sensor sends a blocking signal. Accordingly, the bus instantaneous elements are not blocked and the main breaker relay may trip. Coordination of instantaneous elements between the feeder relays and the main breaker relay is achieved by setting a time delay of a few cycles on the instantaneous elements of the main breaker relay.

Review

- Why are switchable buses difficult to protect?
- What are the differences between bus high- and low-impedance differential protection schemes?
- What is a fast bus tripping scheme?

Summary

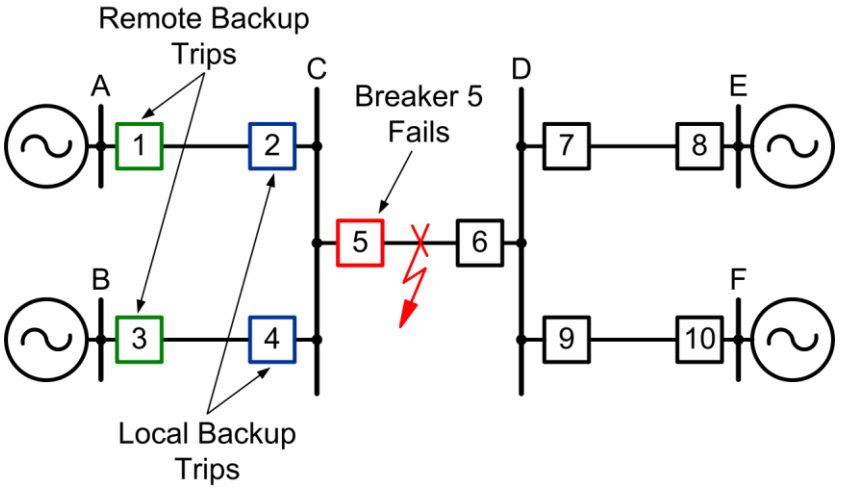
- ☑ Bus configuration influences bus protection scheme selection and design
- ☑ Bus protection schemes should provide high security for external faults
- ☑ High-speed tripping is intended to improve human safety, system transient stability, and power quality; it also reduces through-fault duty on network elements

Breaker failure protection

Dependable protection requires redundant primary protection systems, complemented with backup protection systems. Breakers are almost never redundant because of their high cost. To address the failure of a breaker to clear a fault, you can apply a dedicated breaker failure protection scheme when it is not acceptable to rely solely on time-delayed backup from relays on adjacent zones.

Breaker failure protection provides faster fault clearing, which improves system stability, reduces equipment damage, and improves power quality. Traditionally, only transmission systems used breaker failure protection. However, modern subtransmission and distribution systems also need fast fault clearing. With multifunction relays, we recommend applying breaker failure protection throughout the power system.

Local vs. remote backup protection



The figure shows the one-line diagram of a power system and helps illustrate the concept of backup protection. For a fault at CD, Breakers 5 and 6 should operate as the primary protection. If Breaker 5 fails to operate, there are two possibilities for removing the contribution from A and B: open Breakers 1 and 3 or open Breakers 2 and 4.

Breakers 1 and 3 are located in remote substations. Relying on them alone is remote backup protection. An advantage of remote backup protection is low cost. The remote backup protection is part of the protection equipment that is needed for primary protection functions of adjacent system elements. Additional investment in equipment is not needed.

Breakers 2 and 4 can provide local backup protection. They are located in the same substation. Local backup protection is more expensive than remote backup because it needs additional equipment. The advantages of local backup over remote backup are greater sensitivity, greater selectivity, and faster operating speed.

Backup protection requires a time delay for proper coordination. The primary protection must be given the opportunity to operate before allowing the backup protection to operate.

Why apply breaker failure protection?

Selectivity Sensitivity Speed

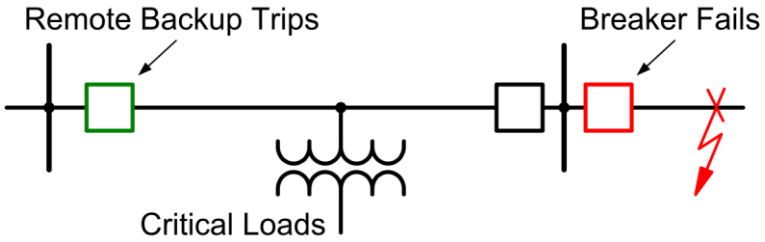
Breaker failure relaying is one form of local backup protection. Consider using breaker failure relaying instead of remote backup if any of the following conditions are true:

- Critical loads, which can be maintained using local breaker failure relaying, are lost due to remote fault clearing
- Remote fault clearing may be sequential, requiring the local fault contribution to be cleared before remote relaying can detect the fault
- Remote backup fault clearing time is greater than maximum allowed fault clearing time due to system stability or equipment damage considerations

Selectivity

Remote backup may cause loss of critical loads in adjacent circuits

Local backup solves this problem



When evaluating whether to rely upon remote backup or to apply local backup, determine if additional loads can be maintained in service by using local backup.

For example, if there are critical loads tapped off of an adjacent line, service can be maintained to these loads by applying breaker failure protection and tripping the adjacent breaker directly instead of relying upon remote relays to clear the fault.

Sensitivity

Remote relays may not reliably detect faults on all adjacent zones

- Radial systems
- Networked systems
  - Infeed limits sensitivity
  - Susceptibility to load encroachment and power swings limits relay Zone 3 settings

The upstream relays may not be set to see past the next fault interruption device.

- With radial systems, this is relatively easy. The limitation is usually on circuit loading
- Networked systems:
  - Infeed limits sensitivity beyond the remote bus
  - There is concern with long reach settings on Zone 3 relays due to susceptibility to load encroachment and power swings

Later we will see how the application of breaker failure protection can help by removing infeed.

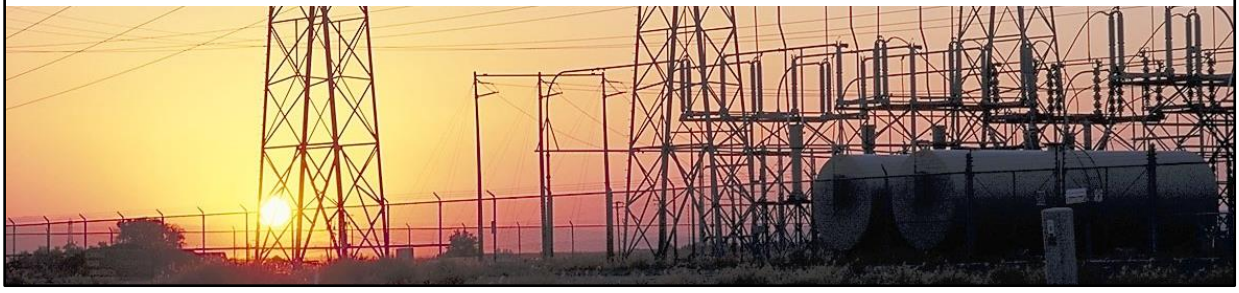
Speed

- Remote backup relays must coordinate with slowest adjacent zone relay
- Breaker failure protection provides faster fault clearing
  - Enhances human safety
  - Improves power system stability
  - Reduces equipment damage
  - Improves power quality

Breaker failure protection provides faster fault clearing, which improves human safety and system stability, reduces equipment damage, and improves power quality.

Additional considerations

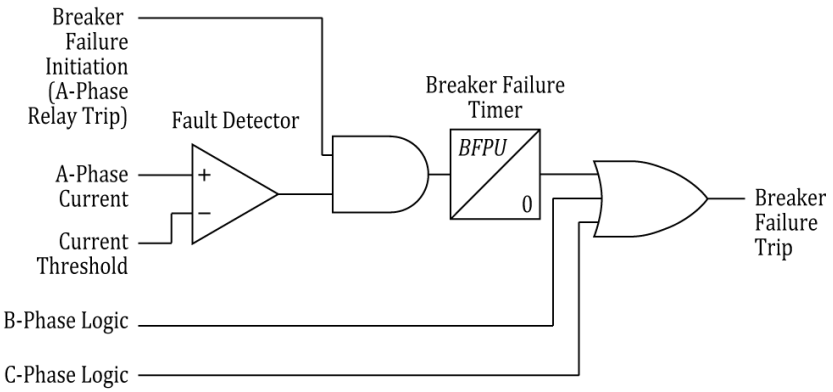
- As the system changes, overlap for backup also changes
- Ease of analysis and maintenance of coordination settings
- Burden of analysis and maintenance of coordination settings is reduced



As the system changes, fault current levels and the distribution of infeed currents change. This will affect the careful analysis of overlap and coordination settings that are required if you are going to rely upon remote backup exclusively.

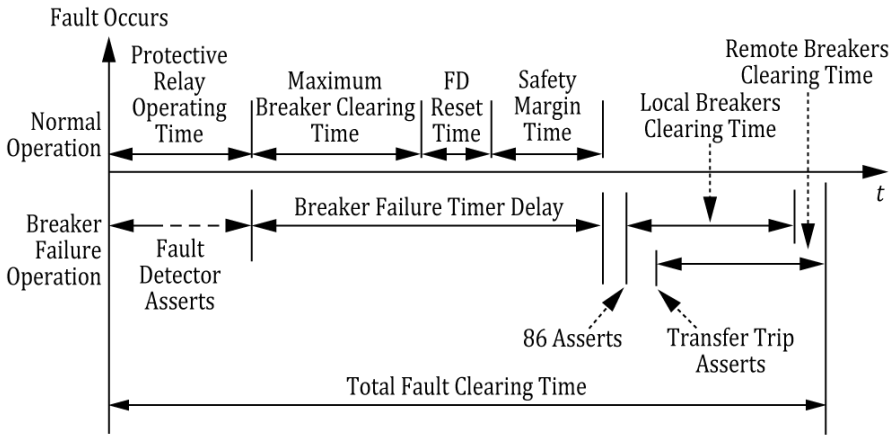
Local breaker failure protection reduces the burden of analysis and maintenance of the remote backup settings. This minimizes the need to consider its coverage of adjacent zones.

Basic breaker failure scheme



The figure depicts the logic for the basic breaker failure protection scheme. During a fault, the primary relay operation provides the breaker failure initiation signal; the fault detector also asserts. The AND output asserts, and the breaker failure timer starts. if the breaker failure initiation input and the fault detector remain asserted until the breaker failure timer expires, the scheme declares a breaker failure and initiates backup breaker tripping. The backup breakers are all the local breakers and all the remote breakers (if transfer trip is available) that must trip to clear the fault when the breaker fails. The scheme resets when the breaker failure initiation input or the fault detector drops out.

Basic breaker failure scheme time chart



The figure shows a time chart for a basic breaker failure scheme. The timer starts when the breaker failure initiation and the fault detector assert. Past approaches used a breaker failure initiation auxiliary relay because proper design requires that the protective relay circuit be isolated from the breaker trip circuit and the breaker failure circuit. However, using an auxiliary relay introduces a small delay before the breaker failure timer starts timing. Today, you can program the output contacts of microprocessor-based relays to directly trip the breaker and also initiate breaker failure timing.

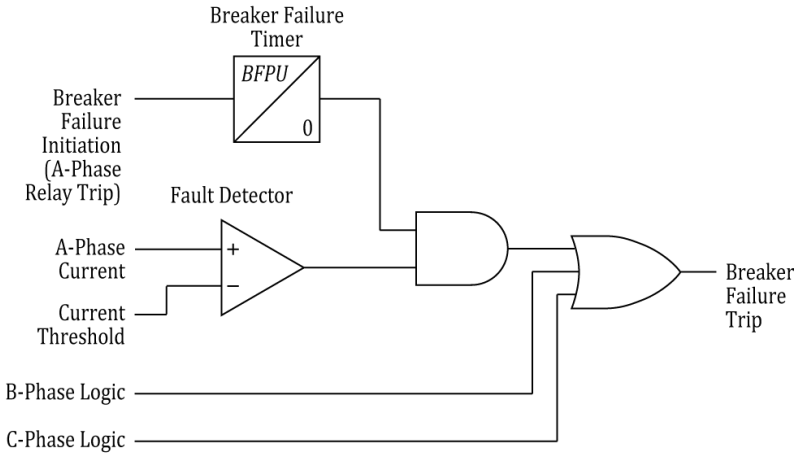
Set the breaker failure timer delay equal to the sum of the maximum breaker clearing time, the time it takes for the fault detector to reset, and a safety margin. In the past, this safety margin allowed for uncertainty in the following parameters:

- Breaker mechanism and interrupter time
- Operating times of the auxiliary relays for primary protection tripping and breaker failure initiation
- Reset time of the fault detector once the breaker successfully interrupts the current
- Timer accuracy

With microprocessor-based relays, timer accuracy and auxiliary relay operating times are no longer a consideration. Later we will discuss the fault detector reset time.

For an actual breaker failure, total fault clearing time also includes the lockout relay (86) operating time (if used) and backup breakers' clearing time. You may also need to transfer-trip remote breakers to clear the fault and issue autoreclose blocking signals to these breakers.

Breaker failure scheme for multibreaker applications

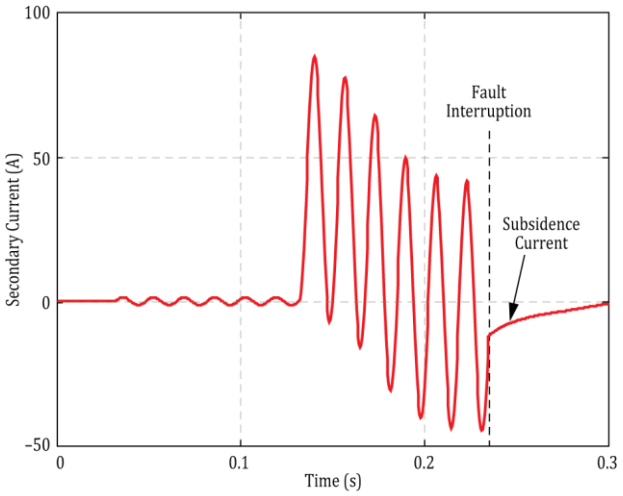


The basic scheme described earlier is applicable for single-breaker bus arrangements. In configurations where two breakers must operate at one terminal to clear a line fault, the current divides between the two breakers, which may cause the fault detectors in one or both relays to fail to pick up. In this case, the breaker failure timer will not start until the first breaker opens successfully and the current redistributes so that all of the current flows through the failed breaker. This delayed timer start causes the breaker failure scheme to trip backup breakers more slowly than intended.

The basic scheme is also susceptible to CT saturation problems. The secondary current dip resulting from CT saturation may cause the fault detector to drop out until the CT recovers from the asymmetrical fault current. The resulting temporary reset of the breaker failure timer increases the breaker failure delay.

In the scheme shown in this figure, the breaker failure timer starts upon assertion of breaker failure initiation only. Therefore, the timer operation is not affected if the fault detector picks up late because of current distribution or drops out because of CT saturation. If current flows through the breaker after the breaker failure timer expires, the breaker failure trip asserts. Use this scheme with caution if the fault detectors are not set above load. The timer will expire if an open breaker has a standing breaker failure initiate. As soon as the breaker closes, the fault detector can pick up and cause immediate breaker failure tripping. The standing initiate can result from a testing error, a circuit problem, or a spurious, remote direct transfer trip (DTT), for example. Section 6.5.7 of *Modern Solutions for Protection, Control, and Monitoring of Electric Power Systems* (see Slide 1 notes for details) describes a solution to this problem.

Subsidence current

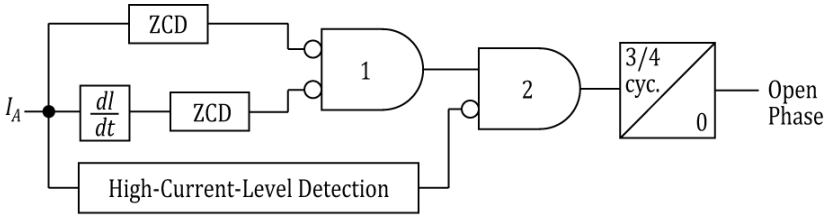


In breaker failure schemes, it is important to detect as quickly as possible not only the pickup but also the dropout of fault-detecting overcurrent elements. Half-cycle cosine filters are often used in these elements to accelerate their pickup and dropout. However, dropout can be delayed by a phenomenon called CT subsidence current. As the figure shows, this current may appear as a small, exponentially decaying dc current with a fairly long time constant. The subsidence current may cause the half-cycle cosine filter to create artificial phasor magnitudes large enough to delay the fault detector reset by some fraction of a cycle. This, in turn, delays detection that the primary ac current has been interrupted. As a result, longer time coordination intervals must be used in the breaker failure logic to preserve security.

Some modern relays, including most dedicated breaker failure relays, use fast open-phase detectors to quickly detect current interruption by examining raw sample data instead of filtered data.

Fast open-phase detector

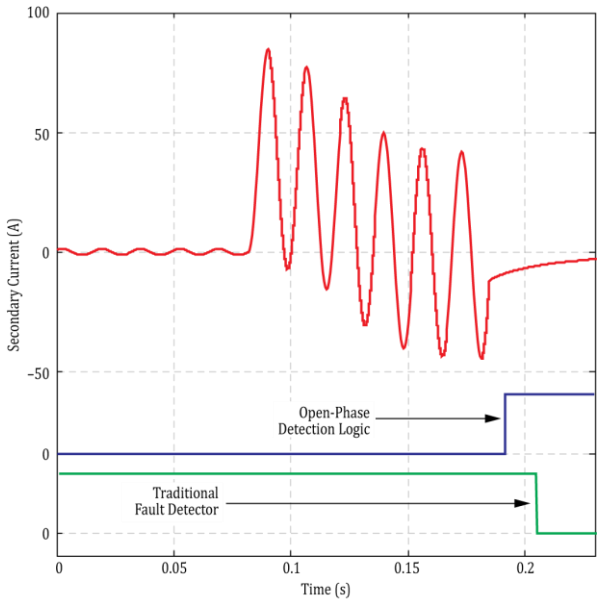
- Supervise breaker failure logic
- Examine raw data instead of filtered data for subcycle detection



As mentioned earlier, an overcurrent element does not reset immediately after the fault current interruption. Fast open-phase detectors can be used to quickly detect current interruption by examining raw sample data instead of filtered data.

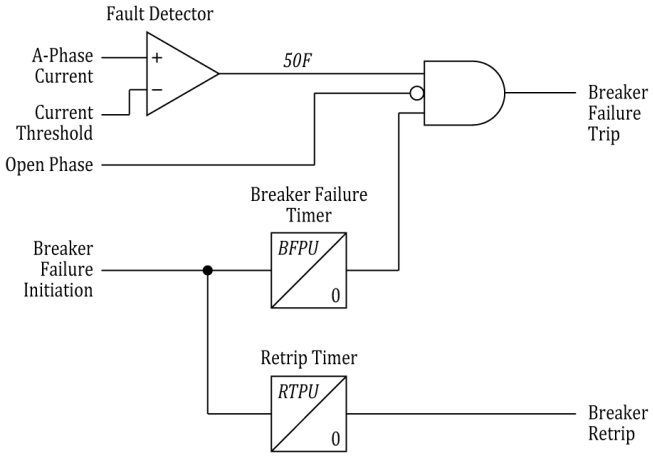
The figure shows a logic that detects an open-phase condition in less than one cycle. The open-phase output supervises the relay breaker failure logic. The logic includes zero-crossing detection (ZCD), the application of which is based on the understanding that a sinusoidal current changes direction and crosses the zero line every half cycle, while a current that contains a decaying dc component takes longer to cross the zero line. However, testing the signal every half cycle is not often enough to detect an open-phase condition in less than one cycle. Hence, a signal slope (*di*/*dt*) evaluation is added to the scheme to detect the minimum and maximum values of the current signal. This evaluation provides an additional measurement between two zero-crossings and enables the relay to detect an open-phase condition in less than one cycle. To increase security, a high-current-level detector is added to ensure correct scheme operation for fictitious zero-slope conditions resulting from analog-to-digital (A/D) converter clipping. The timer time delay *TPU* is less than one cycle.

Fast open-phase detector operation



The figure on the slide shows the difference in open-phase detection time between the fast open-phase detection logic and the traditional fault detector. The positive output of the open-phase detection logic indicates its assertion (open-phase detection). The zero output of the traditional fault detector indicates its reset (open-phase detection). The figure shows that the open-phase detection logic is faster than the traditional fault detector for detecting subsidence current conditions and classifying them as open-phase conditions.

Breaker failure scheme with open-phase detection supervision



The supervision provided by the open-phase detection algorithm facilitates faster overall breaker failure operation times by reducing the reset time margin. The efficacy of the open-phase detection algorithm prevents erroneous breaker failure scheme operation due to subsidence current.

The fast-reset breaker failure protection scheme with consistent delay shown in the figure improves overall system stability margins by reducing the time in which the system is exposed to the faulted bus or line, after at least one breaker fails. In this scheme:

- The top input to the AND gate is output *50*F of the fault detector
- The middle input to the AND gate is the open-phase detector output. This input allows you to improve the system stability margin by applying a shorter breaker failure delay than would be possible with a traditional fault detector
- The bottom input to the AND gate is the output of the breaker failure timer, which starts when initiated by the primary relays

The scheme shown in the figure also includes a retrip function, which issues a tripping signal to the failed breaker before the breaker failure timer expires. If the trip is successful, the open-phase detector asserts and prevents a breaker failure trip from opening all the backup breakers. The retrip function enhances security. If the fault detector is set below the load current and a sustained, spurious initiation signal starts the breaker failure logic, the retrip function trips only one breaker instead of tripping all backup breakers. A short retrip delay *RTPU* could be added. However, this delay must be considered when you are determining the breaker failure timer pickup *BFPU*.

Breaker failure tripping considerations

Single-bus applications

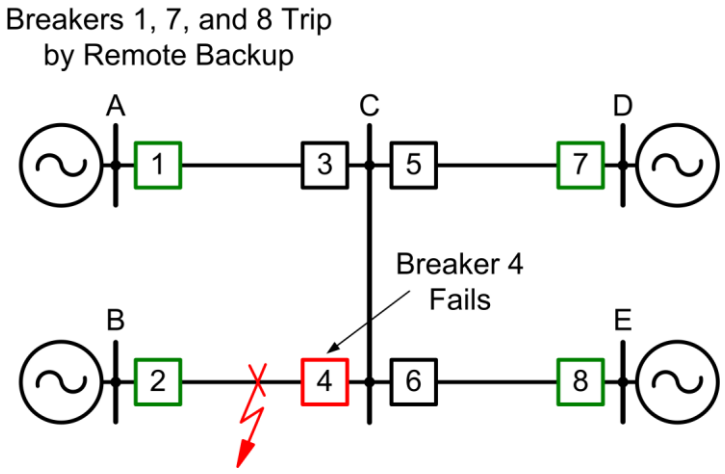
Multibreaker bus applications

It is common practice to use a lockout relay (86) for breaker failure tripping. Breaker failure schemes use either the 86B bus lockout relay with appropriate breaker failure targeting or a dedicated 86BF lockout relay. The lockout relay provides contact multiplication to trip all the backup breakers.

However, modern relays with many programmable contacts and/or protection communications links for tripping adjacent breakers make the lockout relay unnecessary. The breaker failure scheme can directly trip the adjacent breakers. Taking the lockout relay out of the critical tripping path improves reliability and speed.

In many cases, the breaker failure scheme requires tripping one or more remote breakers to completely isolate the faulted section. Remote backup protection can trip the remote breaker(s). When a communications channel is available, the breaker failure scheme can send a DTT signal to the remote breaker(s). This signal can also be used to block remote breaker reclose.

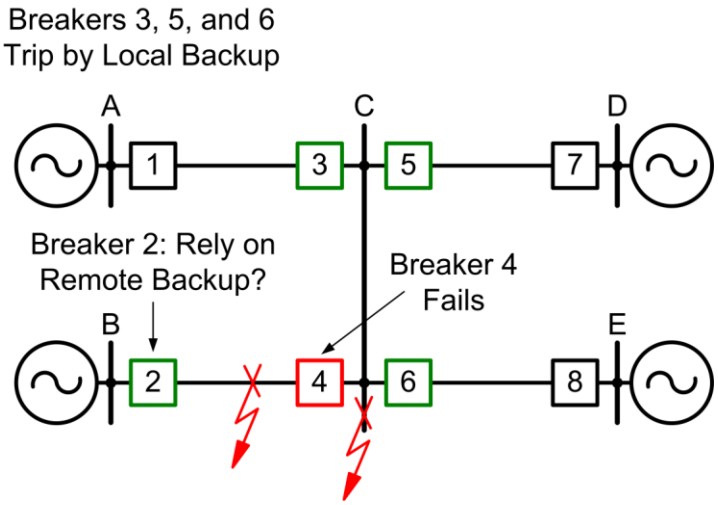
Single-bus applications



Consider the application of remote backup to the power system shown in the figure. In this example, assume that pilot protection has not been applied because stability is not a concern in this region of the power system. If, for the fault shown, Breaker 4 fails to trip, Relays 1, 7, and 8 would have to cover 100 percent of line BC. When infeed is considered, the Zone 3 relays at these remote terminals would have to have extremely long reach settings. Long reach settings are more susceptible to power swings or load encroachment.

If breaker failure protection is applied for local backup, you do not have to rely upon those relays at all.

Single-bus applications



Now, consider the application of a breaker failure protection system to the power system shown in the figure. Breaker 4 will be called upon to trip for faults on two power system elements:

- Fault on Line BC (Breakers 2 and 4 should trip)
- Fault on Bus C (Breakers 3, 4, 5, and 6 should trip)

If Breaker 4 fails to trip, Breakers 3, 5, and 6 are tripped and locked out by the breaker failure protection system.

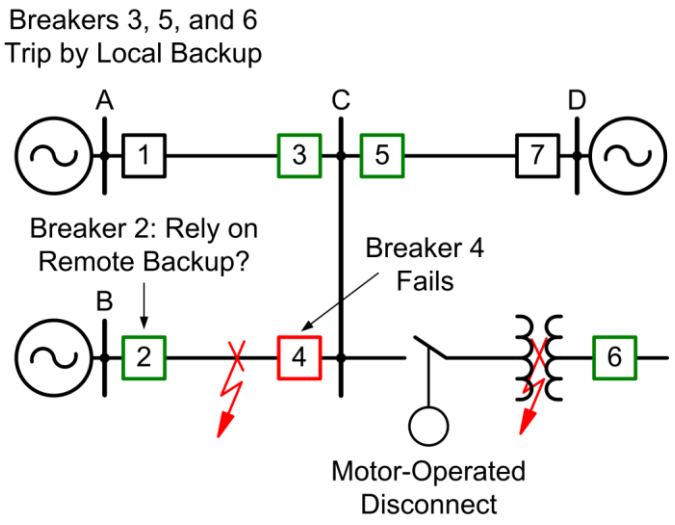
The only breaker to consider for both faults is Breaker 2 at Substation B. The local backup can send a DTT signal if a teleprotection channel is available. Or remote backup can be relied upon to supplement local backup protection for this breaker.

Consider each fault in turn:

- Fault on Line BC: Breaker 2 trips normally. There is no concern with sensitivity.
- Fault on Bus C: Breaker 2 trips in Zone 2. There is no concern with sensitivity. Adding a DTT system can speed clearing and prevent autoreclose of Breaker 2.

Notice that in straight bus applications, for any breaker failure, all breakers around the bus can be tripped.

Single-bus applications



Consider the application of a breaker failure protection system to the power system shown in the figure. In this case, the transformer breaker has been replaced with a motor-operated disconnect (MOD) switch. Breaker 4 will be called upon to trip for faults on three power system elements:

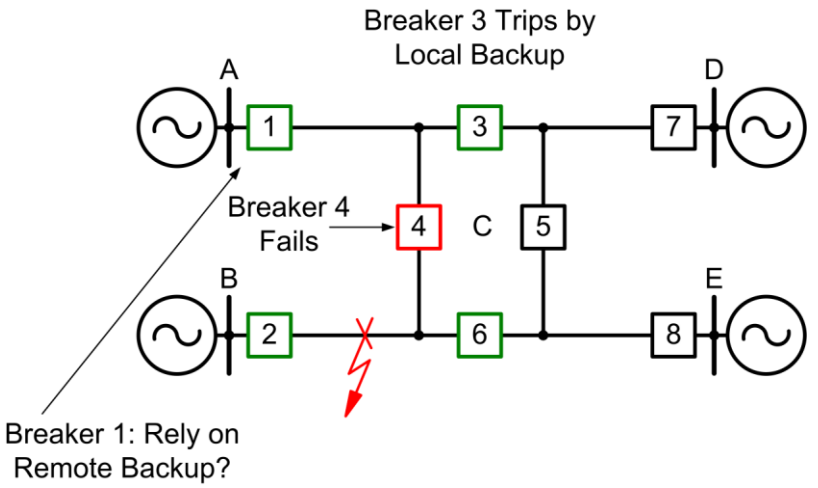
- Fault on Line BC
- Fault on Bus C
- Fault in the transformer (Breakers 3, 4, 5, and 6 are tripped, the MOD is opened, and the breakers are reclosed)

Consider what would happen if Breaker 4 fails for a transformer fault. Breakers 3, 5, and 6 are locked out by the breaker failure protection system.

Breaker 2 at Substation B is again the concern. The local backup can send a DTT signal if a teleprotection channel is available. Or remote backup can be relied upon to supplement local backup protection for this breaker.

For the transformer protection zone, relays at Breaker 2 may not have the necessary sensitivity to detect all the faults that are detected by the sensitive transformer protection. In this case, local backup via DTT would improve the application. Otherwise, the MOD is sacrificed and is used to clear the fault. The MOD would not be interlocked with Breakers 3, 4, and 5 and would open under fault. This would cause a flashover and a bus fault that could be seen by the relays at Breaker 2. This approach considers the probabilities that transformer faults are rare and that a breaker failure is even rarer. However, in this case, damage would be extensive.

Multibreaker bus applications



Ring-bus and breaker-and-a-half arrangements require tripping multiple breakers, including remote breakers, to completely isolate the faulted section. Consider Breaker 4 on the Substation C ring bus shown in the figure.

- For a fault on Line BC, the line primary protection trips Breakers 2, 4, and 6.
- If Breaker 4 fails to trip:
  - Breakers 2 and 6 are already open from the original trip.
  - The breaker-failure scheme trips Breaker 3, which removes the current contributions from Substation D and Substation E.
  - The remote backup protection trips Breaker 1 at Substation A.

The backup relays at Breaker 1 (Distance Zone 3, for example) must have enough sensitivity to cover 100 percent of Line BC or Line CD if we consider the failure of Breaker 3. The removal of infeed by local breaker-failure protection facilitates fault detection by Breaker 1 relays. A better alternative, when a communications channel is available, is a DTT of Breaker 1 initiated by the breaker-failure scheme. Transfer trip reduces fault-clearing time to breaker-failure time and eliminates the reliance on Zone 3 reach.

Review

- Compare remote and local backup in selectivity, sensitivity, speed, and cost
- Describe operation of breaker-failure protection schemes
- Why is attempting to retrip the breaker important?

Summary

- ☑ Declare breaker failure following
  - Breaker failure initiation as primary relays attempt to trip associated breakers for fault
  - Breaker fails as indicated by current still flowing through the breaker after its complete interruption time elapses
- ☑ Apply one breaker failure scheme per breaker in all bus configurations; block autoreclosing of adjacent breakers

Summary

- ☑ Breaker failure scheme should attempt to retrip failed breaker before tripping all adjacent breakers
- ☑ When breaker is undergoing maintenance or test, breaker failure scheme should be disabled to prevent unintentional tripping of station

Questions?